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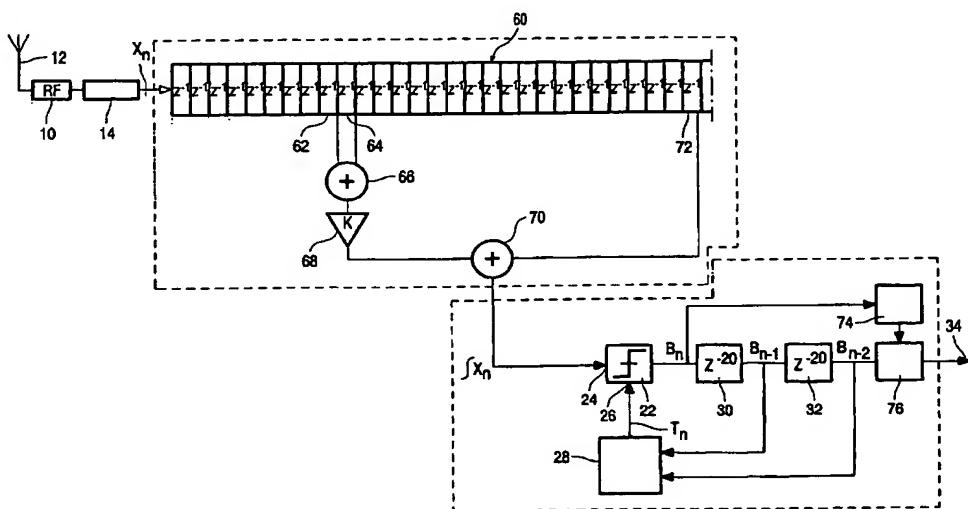
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(54) Title: FSK RECEIVER HAVING A VARIABLE THRESHOLD SLICER STAGE AND CORRESPONDING METHOD



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(57) Abstract: A receiver having a variable threshold slicer stage, comprises a demodulator (14) for providing asynchronously samples of over-sampled raw demodulated data, a shift register (60) for delaying the over-sampled data by up to 2 bit periods. Samples in stages (62, 72) corresponding to substantially the mid-points in two successive bit periods are combined to form a signal (fX_n) to be applied to a bit slicer (22). A bit stream signal from the bit slicer (22) is delayed by two concatenated shift registers (30, 32) for 2 bit periods and is contemporaneously applied to a clock recovery circuit (74) for producing clock signals at the data rate for sampling the delayed sliced signal (Bn-2) at the center of bit to produce an output signal (34).